This listing replaces all prior versions, and listing of claims in the application:

1.   (currently amended) A process for controlling a multiple core expander comprising:

      using a test port of said multiple core expander to ~~send~~ receive operational codes including a dummy bit from a host computer into a multi-bit shift register and a single bit shift register to said multiple core expander to put all but one core expander of said multiple core expander in bypass mode;

      decoding the operational input codes by a state machine of the core expander not placed in bypass mode;

      serially reading data from, and serially writing data to, at least one internal register of said one core expander not placed in bypass mode ~~through said test port~~ by the state machine~~.~~; and

      the state machine inputting a control signal to a multiplexer to shift data to the output port of the core expander not placed in bypass mode to either a series connected core expander or back to the host computer.

2.   (currently amended) A method of controlling the operation of a dual expander having a first expander core and a second expander cores by reading and writing control bits through a single test port in said dual expander comprising:

      placing one of said first expander core and said second expander cores in bypass mode utilizing a single bit shift register;

      transmitting a serial data stream of said control bits through said test port to a shift register to generate a control byte for the expander core that is not in bypass mode;

      parallel shifting said control byte from said shift register to a ~~control~~ single bit shift register in one of said first expander core and said second expander cores that is not in bypass mode;

providing dummy bits ~~as needed~~ in said serial data stream to correctly form said control byte <u>for the expander core that is not in bypass mode</u>.

3.   (currently amended) A process for performing a register write operation in a first expander core of a dual expander comprising:

serially shifting operational code bits into a test port, said operational code bits including instructions <u>with a dummy bit from a host computer into a multi-bit shift register and a single bit shift register</u> to place ~~a~~ <u>the</u> second expander core, in said dual expander, in bypass mode;

generating an operational byte from said operational code bits;

placing said second expander core in bypass mode in response to said operational byte;

~~shifting a dummy bit into said test port;~~

serially shifting control bits, address bits and write command bits into said test port;

<u>reading the serially shifted control bits, address bits and write command bits by a state machine;</u>

generating a control byte <u>by the state machine</u> from said control bits and an address byte from said address bits;

writing said control byte <u>by the state machine</u> to a register in said first expander core at an address indicated by said address byte.

4.   (currently amended) A process for performing a register write operation in a second expander core of a dual expander comprising:

serially shifting operational code bits into a test port of said dual expander, said operational code bits including instructions <u>with a dummy bit from a host computer into a multi-bit shift register and a single bit shift register</u> to place ~~a~~ <u>the</u> first expander core, in said dual expander, in bypass mode <u>utilizing a single bit shift register</u>;

generating an operational byte from said operational code bits;

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placing said first expander core in bypass mode in response to said operational byte;

shifting control bits, address bits and write command bits into said test port;

~~shifting a dummy bit into said test port;~~

<u>reading the serially shifted control bits, address bits and write command bits by a state machine;</u>

generating a control byte <u>by the state machine</u> from said control bits and an address byte from said address bits;

writing said control byte <u>by the state machine</u> to a register in said second expander core at an address indicated by said address byte.

5. (currently amended) A process for performing a register read operation from a first expander core of a dual expander comprising:

serially shifting operational code bits into a test port of said dual expander, said operational code bits including instructions <u>with a dummy bit from a host computer into a multi-bit shift register and a single bit shift register</u> to place ~~a~~ <u>the</u> second expander, in said dual expander, in bypass mode;

generating an operational byte from said operational code bits;

placing said second expander core in bypass mode in response to said operational byte;

~~shifting a dummy bit into said test port of said dual expander;~~

serially shifting read address bits and a read command into said test port of said dual expander;

generating an address byte <u>by a state machine</u> from said read address bits;

serially reading data <u>by a state machine</u> from a register in said first expander core at an address indicated by said address byte through said test port of said dual expander.

6.   (currently amended) A process for performing a register read operation from a second expander core of a dual expander comprising:

serially shifting operational code bits into a test port of said dual expander, said operational code bits including instructions <u>with a dummy bit from a host computer into a multi-bit shift register and a single bit shift register</u> to place a <u>the</u> first expander, in said dual expander, in bypass mode;

generating an operational byte from said operational code bits;

placing said first expander core in bypass mode in response to said operational byte;

serially shifting read address bits and a read command into a test port of said dual expander;

~~shifting a dummy bit into said test port of said dual expander;~~

generating a read address byte <u>by a state machine</u> from said read address bits;

serially reading data <u>by a state machine</u> from a register in said second expander core at an address indicated by said address byte through said test port of said dual expander.